REMARKS

Applicant thanks the Examiner for indicating that claims 9-14 are allowable and for indicating that claims 22, 25 and 28-30 contained allowable subject matter. Applicant also acknowledges the Examiner's suggestion to resubmit the IDS statements filed on December 31, 2001 and May 7, 2001 to eliminate confusion as to whether the IDS statement filed on December 31, 2001 has been considered. Both IDS statements are submitted with this response for the Examiner's consideration. Applicants respectfully requests consideration of the IDS statements.

I. Introduction

Claims 9-14, 18 and 21-36 are pending in the above application.

Claims 18, 21, 23, 24, 26 and 27 stand rejected under 35 U.S.C. § 103.

Claims 31-36 are newly added.

Claims 9-14 stand allowed and claims 22, 25 and 28-30 are indicated to contain allowable subject matter.

Claims 9, 11, 18 and 23 are the independent claims.

II. Amendments

Claims 19-20 have been canceled without prejudice or disclaimer. Accordingly, the rejections thereon are believed to be moot.

Claims 9-12 have been amended to improve clarity and grammar. The scope of claims 9-12 has not been changed by these amendments.

Claims 18, 21, 22, 23, 24, 25, 26, 28, 29 and 30 have been amended to more particularly and distinctly recite what Applicant regards as the invention therein. Support for the

amendments to claims 18, 21, 23 and 24 may be found at least at page 20, line 20 to page 25, line 5 and page 26, line 19 to page 26, line 26 of the specification, and Figs. 1 and 2; claims 22 and 25 at page 37, line 1 to page 40, line 17 and Figs. 7 and 8; claim 26 at page 23, line 25 to page 24, line 3 and Fig. 2; and claims 27-36 at page 27, line 6 to page 36, line 25 and Figs. 4 and 5.

Claims 31-36 are newly added.

No new matter has been added.

III. Prior Art Rejections

A. Claim 18 stands rejected under 35 U.S.C. § 103 as being unpatentable over Sasaki et al (U.S. Pat. No. 6,211,849) (hereafter "Sasaki").

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *Ecolochem Inc. v. Southern California Edison Co.*, 227 F.3rd 1361, 56 U.S.P.Q.2d (BNA) 1065 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2D (BNA) 1614, 1617 (Fed. Cir. 1999); *In re Jones*, 958 F.2d 347, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992); and *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). See also MPEP 2143.01.

Sasaki does not disclose or suggest a liquid crystal driving circuit having a plurality of source driver circuit devices and a plurality of in-chip reference voltage wires, each in-chip reference voltage wire directly connecting each input-side pad to each output-side pad to transmit the reference voltage, as recited by amended claim 18. As the Office action acknowledges, Sasaki discloses that each inter-module wiring 10 connects the input pad portion

2 of one driver IC of the two adjacent driver ICs 1 with the output pad portion 3 of the other driver IC (see Fig. 3). Moreover, Sasaki discloses that the device includes the plurality of buffers 4 receiving the signals (CLK, DATA, CNT) supplied from the input pad portion 2 and the plurality of buffers 8 outputting the signals (CLK, DATA, CNT) to the output pad portion 3. However, Sasaki fails to disclose or suggest a plurality of in-chip reference voltage wires connecting directly an input pad portion 2 with an output pad portion 3 on one driver IC 1. Sasaki merely discloses that the plurality of buffers 4, 8 are inserted into the inter-module wirings 10 in series.

According to the liquid crystal driving circuit recited in the amended claim 18, it is possible to reduce the total cost of the liquid crystal display device by omitting the wires for supplying reference voltages on the first wiring substrate 10.

Moreover, each buffer connected to each branch reference voltage wire prevents the current from flowing to each branch reference voltage wire, and thereby voltage drop can be prevented in the plurality of in-chip reference voltage wires connecting directly an input-side pad unit with an output-side pad unit. Therefore, visual disadvantages, such as parti-color of the liquid crystal elements, can be prevented.

Accordingly, as Sasaki does not disclose or suggest every element of amended claim 18, Sasaki does not produce the claimed invention therein and does not render claim 18 unpatentable.

B. Claim 21 stands rejected under 35 U.S.C. § 103 as being unpatentable over Sasaki in view of the admitted prior art (hereafter "APA").

The addition of APA to Sasaki does not cure the deficiencies of Sasaki with respect to independent claim 18, from which claim 20 depends and hence incorporates all of the limitations thereof. APA discloses that the plurality of reference voltage wires 131 are branched off from the wires formed on the first wiring substrate 110 wherein the plurality of reference voltages supplied from the plurality of reference voltage wires 131 are input to the reference voltage production resistor section 132 via the pad 133 (see Figs. 10 and 11 of the present application). The reference voltage production resistor section 132, as described in the present specification, produces further subdivided reference voltages (e.g., 64 steps) by a resistance voltage divider when a plurality of reference voltages are supplied. The reference voltages are set at, for example, any of the ten steps of voltage values,. In other words, the current supplied through the plurality of reference voltage wires 131 is converted into a plurality of voltage values (e.g., 64 steps) by the reference voltage production resistor section 132. In short, APA fails to disclose or suggest a plurality of buffers each of which is coupled to each branch reference voltage wire.

As discussed above, each buffer connected to each branch reference voltage wire prevents the current from flowing to each branch reference voltage wire, and thereby voltage drop can be prevented in the plurality of in-chip reference voltage wires connecting directly an input-side pad unit with an output-side pad unit. Therefore, visual disadvantages, such as parti-color of the liquid crystal elements, can be prevented.

These effects cannot be obtained by the combination of the cited references and APA. According to the cited references and APA, offset voltage of each buffer connected in series to corresponding one of the plurality of in-chip reference voltage wires, which directly connect an input-side pad unit with an output-side pad unit, and the current flowing through the reference

voltage wires affect the reference voltage. As a result, voltages supplied to liquid crystal elements via the selection circuits from the source driver circuits vary.

Accordingly, as neither Sasaki nor APA, taken alone or in combination, disclose or suggest every element of amended claim 21, the combination of Sasaki and APA does not produce the claimed invention therein and does not render claim 21 unpatentable.

C. Claims 23, 24, 26 and 27 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sasaki in view of Kawaguchi (U.S. Pat. No. 5,670,994).

Neither Sasaki nor Kawaguchi disclose or suggest a liquid crystal driving circuit having a plurality of in-chip reference voltage wires, each in-chip reference voltage wire directly connecting each input-side pad to each output-side pad to transmit the reference voltage, as recited by amended claim 23. Sasaki does not disclose such as discussed above. The addition of Kawaguchi to Sasaki does not cure the deficiencies of Sasaki. As the Office action acknowledges, Kawaguchi discloses that a plurality of ICs are provided for driving the liquid crystal panel wherein the input terminal and the output terminal are directly connected to each other on the IC 229 (see Figs. 31 and 32, and col. 29, lines 38-55). However, Kawaguchi fails to disclose or suggest wires which are branched off from wires connecting directly the input terminal with the output terminal on the IC 229 (wires corresponding to "a plurality of reference voltage wires" recited in the present claims).

Accordingly, as neither Sasaki nor Kawaguchi, taken alone or in combination, disclose or suggest every element of amended claim 23, the combination of Sasaki and APA does not produce the claimed invention therein and does not render claim 23 unpatentable. As claims 24,

26 and 27 depend on amended claim 23, and incorporate all of the limitations thereof, the combination of Sasaki and Kawaguchi also does not render claims 24, 26 and 27 unpatentable.

IV. New Claims

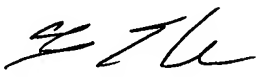
New claims 31-36 are believed to be patentable because they are believed to recite combinations of elements which are not disclosed or suggested by the prior art.

V. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
MCDERMOTT, WILL & EMERY



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